**Supporting Information for *Acta Phys. -Chim. Sin.* 2017**, *33* (1), 249－254
doi: 10.3866/PKU.WHXB201610142

# 基于 $CH_3NH_3PbI_3$ 单晶的 $Ta_2O_5$ 顶栅双极性场效应晶体管

吕乾睿　　李　晶　　廉志鹏　　赵昊岩　　董桂芳*　　李　强
王立铎　　严清峰*

(清华大学化学系，北京 100084)

# $CH_3NH_3PbI_3$ Single Crystal-Based Ambipolar Field-Effect Transistor with $Ta_2O_5$ as the Top Gate Dielectric

**LÜ Qian-Rui　　LI Jing　　LIAN Zhi-Peng　　ZHAO Hao-Yan　　DONG Gui-Fang***
**LI Qiang　　WANG Li-Duo　　YAN Qing-Feng***

(*Department of Chemistry, Tsinghua University, Beijing 100084, P. R. China*)

*Corresponding authors. DONG Gui-Fang, Email: donggf@mail.tsinghua.edu.cn; Tel: +86-10-62782287.
YAN Qing-Feng, Email: yanqf@mail.tsinghua.edu.cn; Tel: +86-10-62792830.

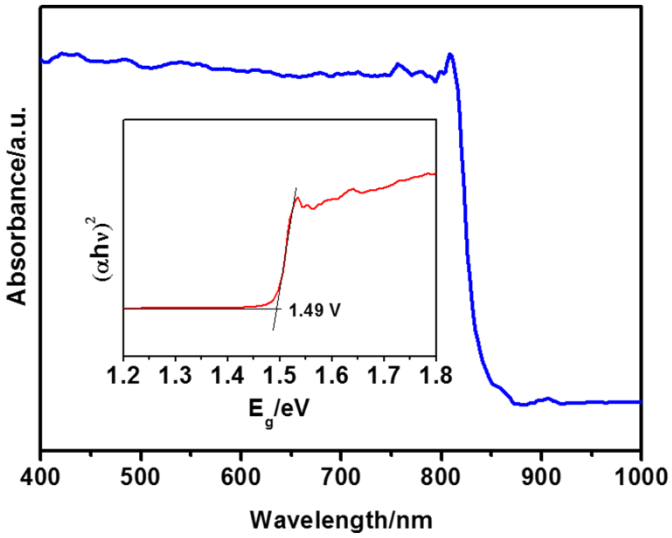


**Fig.S1 UV-visible absorption spectrum of as-prepared $MAPbI_3$ single crystal plate**
The inset shows the band-gap calculation.

Fig.S2 shows $I_{DS}$ reached saturation quickly and the saturation regions of the FET under different $V_{GS}$ were very short. When the $V_{DS}$ reached about 25 V, the FET went into the breakdown region and the device was destroyed.

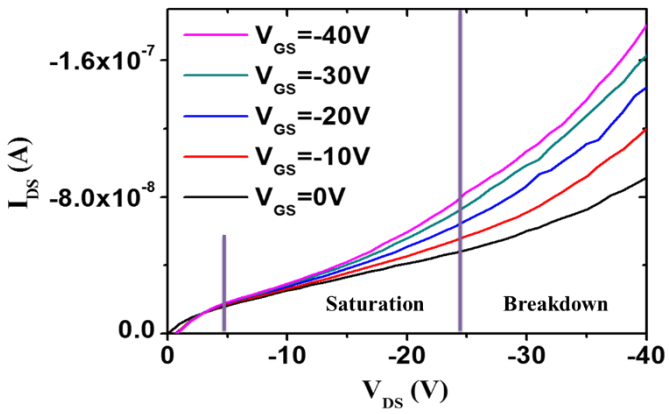


**Fig.S2 Output curves of the FET in the dark condition**

Fig.S3 shows a bottom-gate/top-contact structure FET based on a $CH_3NH_3PbI_3$ single crystal and $SiO_2$ dielectric layer. It was composed of a gate electrode, a gate dielectric, a semiconductor layer, a source electrode, and a drain electrode, from the bottom up. A heavily doped *n*-type Si wafer was used as the gate electrode, with a 300 nm thick thermally oxidized $SiO_2$ layer as the gate dielectric. The fresh $CH_3NH_3PbI_3$ single crystal with two flat opposite exposed surface was

placed on the Si wafer as the semiconductor layer. Au strips of 75 nm in thickness were deposited on the upper flat surface of the single crystal by a conventional thermal evaporation method through a stainless steel mask as source electrodes and drain electrodes. The deposition rate was 0.01 $nm \cdot s^{-1}$ and it is suspended several times during the process to protect the single crystal from overheating. The channel width (W) was 800 μm, and the channel length (L) was 60 μm.

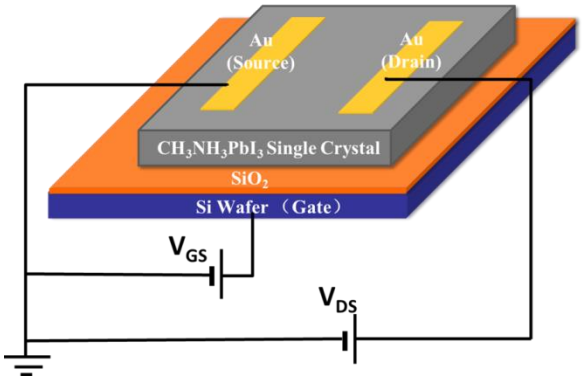


**Fig.S3 Sketch of the bottom-gate/top-contact structure FET based on a $CH_3NH_3PbI_3$ single crystal and $SiO_2$ dielectric layer**

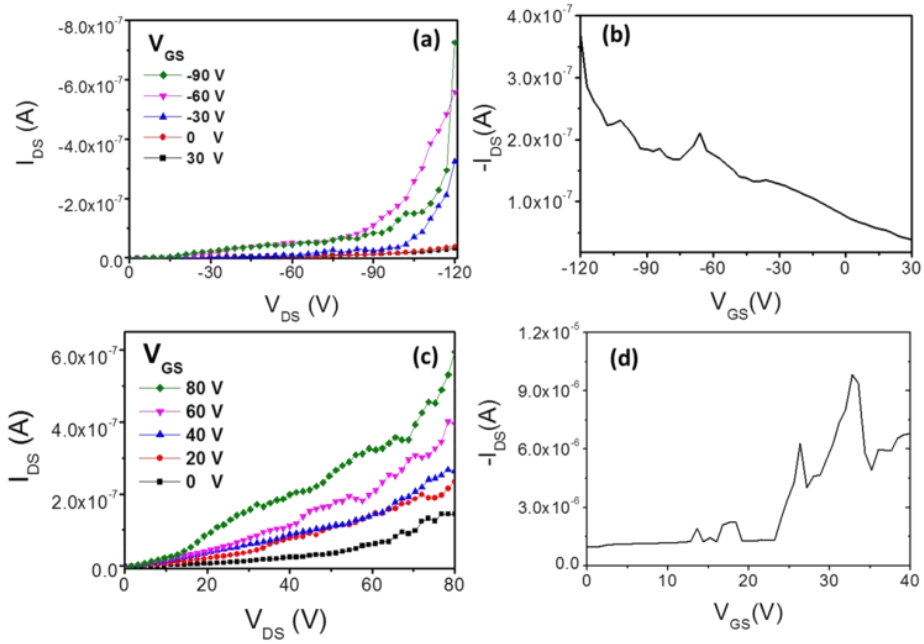


**Fig.S4 FET characteristics of the bottom-gate/top-contact structure $CH_3NH_3PbI_3$ single-crystal FET with the $SiO_2$ gate dielectric layer**

(a) output curves for *p*-type, (b) transfer curve for *p*-type, (c) output curves for *n*-type and (d) transfer curve for *n*-type